REMARKS

This Preliminary Amendment is being filed to correct some typographical errors and to invoke an interference with a patent pursuant to 37 C.F.R. 1.607

(1) IDENTITY OF PATENT

Applicants seek to invoke an interference with **Sasaki et al.**, "METHOD OF DIVIDING A WAFER AND METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE", U.S. Patent 5,888,883 (1999).

(2) PROPOSED COUNTS

The proposed counts are:

COUNT I

A wafer dividing method comprising the steps of:

forming grooves in a surface of a wafer, on which surface semiconductor elements are formed, along dicing lines, said grooves being deeper than a thickness of a finished chip;

attaching a holding member on said surface of the wafer on which the semiconductor elements are formed; and

lapping and polishing a bottom surface of the wafer to said thickness of the finished chip, thereby dividing the wafer into chips,

wherein in the step of dividing the wafer into the chips, the lapping and polishing is continued until the thickness of the wafer becomes equal to the thickness of the finished chip, even after the wafer has been divided into the chips by the lapping and polishing.

COUNT II

A method of manufacturing a semiconductor device, comprising the steps of:

forming semiconductor elements in a major surface of a wafer;

forming grooves in said major surface of the wafer along dicing lines, said grooves being deeper than a thickness of a finished chip;

attaching an adhesive sheet on said major surface of the wafer;

lapping and polishing a bottom surface of the wafer to said thickness of the finished chip, thereby dividing the wafer into chips; and

separating each of the divided chips from the adhesive sheet and sealing said each chip in a package,

wherein in the step of dividing the wafer into the chips, the lapping and polishing is continued until the thickness of the wafer becomes equal to the thickness of the finished chip, even after the wafer has been divided into the chips by the lapping and polishing.

(3) CORRESPONDING CLAIMS IN PATENT

COUNT I

Claims 1, 2 and 3 of Sasaki correspond to Count I. Claim 1 of Sasaki corresponds exactly to Count I. Claims 2 and 3 of Sasaki depend from Claim 1 and correspond substantially to Count I.

COUNT II

Claims 4, 5, 6, 7 and 8 of Sasaki correspond to Count II. Claim 4 of Sasaki corresponds exactly to Count II except that Count II omits the extraneous "a" (first occurrence after "forming") on the third line of Sasaki's Claim 4. Claims 5, 6, 7 and 8 of Sasaki depends from Claim 4 and correspond substantially to Count II.

(4) CORRESPONDING CLAIMS IN APPLICATION

Claims 28, 29, 30, 31 and 32 of this application have been copied from Sasaki claims 1, 2, 3, 4 and 5, respectively, except that Claim 30 identifies only one possible "holding member" whereas Sasaki claim 3 lists several others.

COUNT I

Claims 28, 29 and 30 of the application correspond to Count I. Claim 28 of the application corresponds exactly to Count I. Claims 29 and 30 of the application depend from Claim 28 and correspond substantially to Count I.

COUNT II

Claims 31 and 32 of the application correspond to Count II. Claim 31 of the application corresponds exactly to Count I. Claim 32 depends from Claim 31 and corresponds substantially to Count II.

(5) SUPPORT IN THE SPECIFICATION

The following table shows how applicants' specification supports the newly added claims:

Claim 28	Support
28. A wafer dividing method comprising the steps of:	On p. 3, lines 5-6, the invention is described as a "method for manufacturing a plurality of thinned integrated circuits from a semiconductor wafer ..."
forming grooves in a surface of a wafer, on which surface semiconductor elements are formed, along dicing lines,	Grooves 30 are formed in surface 24 of wafer 20. Dies 34 are formed on surface 24 along streets 30.. See Fig. 2; p. 9, line 24 - p.10, line 26.
said grooves being deeper than a thickness of a finished chip	On p. 10, lines 1-3, each die 34 will ultimately form a separate IC chip. Grooves 30 have a depth 32 equal to or slightly exceeding the final thickness desired for wafer 20 after thinning, i.e. the final thickness of a finished chip.
attaching a holding member on said surface of the wafer on which the semiconductor elements are formed; and	Substrate 10 is attached to surface 24 of the wafer 20 on which the dies 34 are formed. See Fig. 3; p. 11, lines 8-10.
lapping and polishing a bottom surface of the wafer to said thickness of the finished chip, thereby dividing the wafer into chips,	The backside 22 of the wafer 20 is initially ground at a first speed and, subsequently at a slower speed, and then polished with a finer grinding machine until dies 34 are separated from each other. See p. 11, line 20 to p. 12, line 11.
wherein in the step of dividing the wafer into the chips, the lapping and polishing is continued until the thickness of the wafer becomes equal to the thickness of the finished chip, even after the wafer has been divided into the chips by the lapping and polishing	The backside 22 is ground to the point where the dies 34 are individually separated from each other. Since the grooves 30 may have a depth exceeding the final thickness desired for the wafer 20 after thinning, the lapping and polishing is continued even after the wafer has been divided into the chips. See p. 10, lines 2-6, 19-21.

Claim 29	Support
29. The wafer dividing method according to claim 28 wherein a depth of each groove is greater than the thickness of the finished chip by at least 5 μm.	On p. 10, lines 1-3, each die 34 will ultimately form a separate IC chip. Grooves 30 have a depth 32 equal to or slightly exceeding the final thickness desired for wafer 20 after thinning, i.e. the final thickness of a finished chip. On p. 10, lines 19-20, the wafer 20 is preferably thinned to 25 microns. On p. 10, lines 3-6, an example is given where the grooves 30 may have a depth 32 in the range of 10 to 75 microns. In the preferred embodiment, therefore, the grooves 30 may be 50 microns deeper than the thickness of the chip (75 - 25 μm). Thus, the depth 32 of the grooves 30 is at least 5 μm greater than the thickness of the finished chip 34.

Claim 30	Support
30. The wafer dividing method according to claim 28 wherein said holding member comprises a substrate coated with an adhesive material.	The substrate 10 is a holding member for the wafer 20 and is coated with an adhesive material 28. See Fig. 3; p. 10, lines 9-12, p. 11, lines 8-10.

Claim 31	Support
31. A method of manufacturing a semiconductor device, comprising the steps of:	On p. 3, lines 5-6, the invention is described as a "method for manufacturing a plurality of thinned integrated circuits from a semiconductor wafer ..."
forming semiconductor elements in a major surface of a wafer;	On p. 6, lines 24-25, a wafer has integrated circuits formed into its upper surface. Dies 34 are formed on surface 24. On p. 9, line 26, a wafer 20 has integrated circuits formed on surface 24. See Fig. 2.
forming grooves in said major surface of the wafer along dicing lines, said	Grooves 30 are formed in surface 24 of wafer 20. See p. 9, line 24 - p.10, line 26,

grooves being deeper than a thickness of a finished chip;	and Fig. 2. On p. 10, lines 1-3, each die 34 will ultimately form a separate IC chip. Grooves 30 have a depth 32 equal to or slightly exceeding the final thickness desired for wafer 20 after thinning, i.e. the final thickness of a finished chip.
attaching an adhesive sheet on said major surface of the wafer;	In Fig. 3, an adhesive layer 28 is disposed on the grooved surface 24.
lapping and polishing a bottom surface of the wafer to said thickness of the finished chip, thereby dividing the wafer into chips; and	The backside 22 of the wafer 20 is initially ground at a first speed and, subsequently at a slower speed, and then polished with a finer grinding machine until dies 34 are separated from each other. See p. 11, line 20 to p. 12, line 11.
separating each of the divided chips from the adhesive sheet and sealing said each chip in a package,	On p. 12, line 24 to p. 13, line 3, each die is individually separated and removed. On p. 14, lines 10-11, each die 34 is sealed in a package.
wherein in the step of dividing the wafer into the chips, the lapping and polishing is continued until the thickness of the wafer becomes equal to the thickness of the finished chip, even after the wafer has been divided into the chips by the lapping and polishing.	The backside 22 is ground to the point where the dies 34 are individually separated from each other. Since the grooves 30 may have a depth exceeding the final thickness desired for the wafer 20 after thinning, the lapping and polishing is continued even after the wafer has been divided into the chips. See p. 10, lines 2-6, 19-21.

Claim 32	**Support**
32. The method of manufacturing a semiconductor device, according to claim 31, wherein a depth of each groove is greater than the thickness of the finished chip by at least 5 μm.	On p. 10, lines 1-3, each die 34 will ultimately form a separate IC chip. Grooves 30 have a depth 32 equal to or slightly exceeding the final thickness desired for wafer 20 after thinning, i.e. the final thickness of a finished chip. On p. 10, lines 19-20, the wafer 20 is

	preferably thinned to 25 microns. On p. 10, lines 3-6, an example is given where the grooves 30 may have a depth 32 in the range of 10 to 75 microns. Thus, the depth 32 of the grooves 30 is at least 5 μm greater than the thickness of the finished chip 34.

(6) 35 U.S.C. 135(b)

Sasaki et al. issued on March 30, 1999, less than one year before the filing of this amendment, such that applicants need not address the requirements of 35 U.S.C. 135(b).

SUMMARY

Applicants respectfully submit that support for each of the newly added claims is found in the specification as detailed above. Applicants respectfully request that the Examiner declare an interference as the newly added claims were copied in whole or in part from Sasaki et al.

Applicants encourage the Examiner to telephone the undersigned attorney if it appears that a telephone conference would help further this case in any way.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on

March 28, 2000

by Eric Hoover

Signature

March 28, 2000

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